Patent claims

1. A method for picture-in-picture insertion,
wherein a sequence of insertion pictures (Kj=K1,K2,...) decimated by vertical decimation (VD ≥ 1) are read into a memory device (S) and subsequently read out,
wherein the insertion pictures (Kj) read out are inserted into a sequence of main pictures (Hi=H1, H2,...),
wherein the memory device (S) has a storage capacity of less than two insertion pictures (Kj) and is subdivided into memory segments (X,Y,Z;A,B,C,D,E) which are continuously overwritten by the insertion pictures, and
wherein a decision is made as to whether the currently written insertion picture (Kj) or the immediately preceding insertion picture (Kj-1) is read out,
characterized
in that more than one memory segment (X,Y,Z;A,B,C,D,E) of the memory device (S) is required for storing an insertion picture (Kj), and
in that the memory segments (X,Y,Z;A,B,C,D,E) of the memory device (S) are cyclically overwritten by the insertion pictures (Kj) in a predetermined order.

2. The method as claimed in claim 1,
characterized
in that the memory segments (X,Y,Z;A,B,C,D,E) are the same size.

3. The method as claimed in claim 1 or 2,
characterized
in that, in a manner dependent on the ratio of a reading speed of a read pointer to a writing speed of a write pointer and a relative position of the write pointer in a writing area (I,II; I,II,III) holding the currently written insertion picture, a decision is made as to whether the currently written insertion picture

(Kj) or the immediately preceding insertion picture (Kj-1) is read out.

4. The method as claimed in one of the preceding claims,
characterized
in that the memory device has a storage capacity which is (2-1/VD) times the storage capacity required for an insertion picture, where VD is the vertical decimation of the insertion picture.

5. The method as claimed in claim 4,
characterized
in that the memory segments are the same size and the number of memory segments is 2* VD-1, the number of memory segments required for an insertion picture corresponding to the vertical decimation (VD).

6. The method as claimed in claim 5,
characterized
in that a memory segment has a storage capacity of 1/VD times the storage capacity required for an insertion picture and the decision criterion that is applied is whether the last memory segment (II; III) required for the currently written insertion picture is already being written too.

7. The method as claimed in one of the preceding claims,
characterized
in that the insertion pictures (Kj) and main pictures (Hi) are fields of a monitor picture.

8. The method as claimed in one of the preceding claims,
characterized
in that a comparison is made to determine whether a main picture (Hi) and an insertion picture (Ki) to be inserted into the latter have an identical field position, and, in the case of a differing field position, an identical field position is achieved by

address shifting of the main picture (Hi) or of the insertion picture.

9. A circuit arrangement for picture-in-picture insertion, in particular for carrying out a method as claimed in one of claims 1 to 8, having a memory device (S) for storing vertically decimated insertion pictures (Kj=K1, K2, ...), the memory device (S) having a storage capacity of less than two insertion pictures (Kj) and being subdivided into memory segments (X,Y,Z;A,B,C,D,E) which can be continuously overwritten by the insertion pictures (Kj),

having a control device (3) for reading out the vertically decimated insertion pictures from the memory device (S) and for inserting the insertion pictures (Kj) read out into a sequence of main pictures (Hi=H1, H2...), and

having a decision device for deciding whether the currently written insertion picture (Kj) or the immediately preceding insertion picture (Kj-1) is read out,

characterized

in that each memory segment (X,Y,Z;A,B,C,D,E) has a storage capacity of less than one insertion picture (Kj), and

in that the memory segments (X,Y,Z;A,B,C,D,E) of the memory device (S) can be cyclically overwritten by the insertion pictures (Kj) in a predetermined order.

10. The circuit arrangement as claimed in claim 9, characterized

in that the memory segments (X,Y,Z;A,B,C,D,E) are the same size.

11. The circuit arrangement as claimed in claim 9 or 10,

characterized

in that the memory device has a storage capacity which is (2-1/VD) times the storage capacity required for an

insertion picture, where VD is the vertical decimation of the insertion picture.

12. The circuit arrangement as claimed in claim 11, characterized
in that the memory segments are the same size and the number of memory segments is 2* VD-1, the number of memory segments required for an insertion picture corresponding to the vertical decimation (VD).

13. The circuit arrangement as claimed in one of claims 9 to 12,
characterized
in that in a manner dependent on the ratio of a reading speed of a read pointer to a writing speed of a write pointer and a relative position of the write pointer in a writing area holding the currently written insertion picture, the decision device decides whether the currently written insertion picture (Kj) or the immediately preceding insertion picture (Kj-1) is read out.